## REMARKS

The above amendments to the above-captioned application along with the following remarks are being submitted as a full and complete response to the Official Action dated December 22, 2004. Applicants thank the Examiner for taking the undersigned representative's phone calls and providing the relevant information. In view of the above amendments and the following remarks, the Examiner is respectfully requested to give due reconsideration to this application, to indicate the allowability of the claims, and to pass this case to issue.

Status of the Claims

Claims 1-5 and 18-24 are under consideration in this application. Claims 1-4 are being amended, as set forth in the above marked-up presentation of the claim amendments, in order to more particularly define and distinctly claim Applicants' invention. New claims 18-24 are being added to recite other embodiments described in the specification.

All the amendments to the claims are supported by the specification. Applicants hereby submit that no new matter is being introduced into the application through the submission of this response.

Formality Rejection

Claim 3 was rejected under 35 U.S.C. § 112, first paragraph, for claiming subject matter that is not described in the specification in such a way that another person skilled in the art could make and/or use the invention. As indicated, claim 3 is being amended to overcome the 112 rejection. Accordingly, the withdrawal of the outstanding informality rejection is in order, and is therefore respectfully solicited.

Prior Art Rejections

Claims 1-5 were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,212,777 to Gove et al. (hereinafter "Gove"). The prior art reference of McCann Jr. et al. (3,774,165), Ing-Simmons et al. (5,239,654), Gove et al. (5,522,083; 5,613,146; 5,768,609; 6,070,003), and Meeker (6,073,185) were cited as being pertinent to the present application. This rejection has been carefully considered, but is most respectfully traversed.

The semiconductor integrated circuit 1 on a semiconductor chip of the invention (for

example, the embodiment depicted in Figs. 1-2 and 10), the semiconductor integrated circuit 1 comprising: a single instruction multiple data (SIMD) unit 3 conducting a concurrent operation for a plurality of data items; a data buffer 9 connectible to said SIMD unit 3; and

a data transfer control unit 5 for controlling transfer of data for said data buffer 9. The data transfer control unit 5 controls the transfer of data for a subsequent operation of the STMD unit 3 to said data buffer 9 ***from outside of said semiconductor integrated circuit 1*** (e.g., from the external mage memory 17) *in concurrence with* the current operation of said SIMD unit 3 for a plurality of data items read ***from said data buffer 9*** (to internal components, such as registers 41, 42, p. 26, line 22).

In concurrence with the current processing by the SIMD operator 40 of the SIMD unit 3, the data for the subsequent processing is externally transferred to the data buffer 9 . "*The period of time used for the actual DMA transfer becomes invisible in the processing time. As a result, SIMD operation performance of the data processor 1 is increased. The SIMD operator 40 is always in a state in which necessary data with the code extension is prepared for operation.*" This increases operation efficiency of the SIMD operator 40 (Fig. 10; [0073] of Published Applications of United States Patent Application 20020184471. Therefore, the operation of the SIMD unit 3 is not interrupted by the internal transfer of the data to the data buffer 9 ([0013] to [0017]).

Applicants respectfully contend that Gove fails to teach or suggest such a "data transfer control unit 5 controls the transfer of data for a subsequent operation of the STMD unit 3 to said data buffer 9 from outside of said semiconductor integrated circuit 1 in concurrence with the current operation of said SIMD unit 3 for a plurality of data items read from said data buffer 9" as in the invention

Gove only arranges a multiprocessor system as an image and graphics processor. The processor is structured with "n" number of individual processors PP0-PPj all having communication links to "m" number of memories M0-Mj without restriction. A crossbar switch 20 serves to establish the processor memory links. The entire image processor, including the individual processors PP0-PPj, the crossbar switch 20 and the memories 10 are contained on a single silicon chip (Fig. 1). Each processor PP0-PPj can operate to execute the same instruction at the same time (StMD mode) or different instructions at the same time (MIND mode). See Abstract. These "*processors [100-104] are arranged to operate*

*independently from each other from instructions executed on a cycle-by-cycle basis* (col. 2, lines 5-8)" thereby "*changing at least some of the processors from the group of processors from operation in the SIMD operating mode (i.e., executing the same instruction at the same time) to operation in the MIMD operational mode (i.e., executing different instructions at the same time) where each processor of the group operates from separate instructions provided by separate instruction memories* (col. 3, lines 15-20)".

Gove's transfer processor 11 (arguable equivalent of the data transfer control unit 5) transfers data from the external memory 15 (Fig. 2) via a bus 21 (col. 5, lines 35-48) as well as transfer data from its internal memory 10 (arguable equivalent of the data buffer 9) via the crossbar switch 20 to the internal memory 10, and Gove's internal memory 10 also transfers data to the master processor 12 (arguable equivalent of the SIMD unit 3) via the crossbar switch 20. However, Gove's transfer processor 11 (col. 12, lines 31-56) does not concurrently (1) transfer data for a *subsequent* operation of the master processor 12 from outside of chip to internal memory 10, and (2) transfer data for the *current* operation of the master processor 12 for a plurality of data items read from the internal memory *10* (to other internal components).

Applicants contend that neither Gove, nor any other cited reference teaches or discloses each and every feature of the present invention as disclosed in the independent claim 1. As such, the present invention as now claimed is distinguishable and thereby allowable over the rejections raised in the Office Action. The withdrawal of the outstanding prior art rejections is in order, and is respectfully solicited.

Conclusion

In view of all the above, clear and distinct differences as discussed exist between the present invention as now claimed and the prior art reference upon which the rejections in the Office Action rely, Applicants respectfully contend that the prior art references cannot anticipate the present invention or render the present invention obvious. Rather, the present invention as a whole is distinguishable, and thereby allowable over the prior art.

Favorable reconsideration of this application is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance of the above-captioned application, the Examiner is invited to contact the Applicants' undersigned representative at the address and phone number indicated below.

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